# Asian Power Electronics Journal

**PERC, HK PolyU**

Copyright © The Hong Kong Polytechnic University 2019. All right reserved.
No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying recording or any information storage or retrieval system, without permission in writing form the publisher.

First edition Oct. 2019 Printed in Hong Kong by Reprographic Unit
The Hong Kong Polytechnic University

**Published by**

Power Electronics Research Centre
The Hong Kong Polytechnic University
Hung Hom, Kowloon, Hong Kong

**ISSN 1995-1051**

**Disclaimer**

Any opinions, findings, conclusions or recommendations expressed in this material/event do not reflect the views of The Hong Kong Polytechnic University

# Editorial board


## Honorary Editor

Prof. Fred C. Lee Electrical and Computer Engineering, Virginia Polytechnic Institute and State University

## Editor

Victor Electronics Ltd.

## Associate Editors and Advisors

Prof. Philip T. Krien
Department of Electrical and Computer Engineering, University of Illinois

Prof. Keyue Smedley
Department of Electrcial and Computer Engineering, University of California

Prof. Muhammad H. Rashid
Department of Electrical and Computer Engineering, University of West Florida

Prof. Dehong Xu
College of Electrical Engineering, Zhejiang University

Prof. Hirofumi Akagi
Department of Electrical Engineering, Tokyo Institute of Technology

Prof. Xiao-zhong Liao
Department of Automatic Control, Beijing Institute of Technology

Prof. Hao Chen
Dept. of Automation, China University of Mining and Technology

Prof. Danny Sutanto
Integral Energy Power Quality and Reliability Centre, University of Wollongong

Prof. S.L. Ho
Department of Electrical Engineering, The Hong Kong Polytechnic University

Prof. Eric K.W. Cheng
Department of Electrical Engineering, The Hong Kong Polytechnic University

Dr. Norbert C. Cheung
Department of Electrical Engineering, The Hong Kong Polytechnic University

Dr. Edward W.C. Lo
Department of Electrical Engineering, The Hong Kong Polytechnic University

Dr. Martin H.L. Chow
Department of Electronic and Information Engineering, The Hong Kong Polytechnic University

Dr. Chi Kwan Lee
Department of Electrical and Electronic Engineering, The University of Hong Kong

**Publishing Director:**
Prof. Eric K.W. Cheng, Department of Electrical Engineering, The Hong Kong Polytechnic University

**Communications and Development Director:**
Dr. James H.F. Ho, Department of Electrical Engineering, The Hong Kong Polytechnic University

**Production Coordinator:**
Ms. Jinhong Sun, Ms Xiaolin Wang and Mr. Yongquan Nie Power Electronics Research Centre, The Hong Kong Polytechnic University

**Secretary:**
Ms. Kit Chan, Department of Electrical Engineering, The Hong Kong Polytechnic University

# Table of Content

Asian Power Electronics Journal, Vol. 13, No. 2, October 2019

# A Simple and Useful Three-Port Converter for Integrating Renewable Energy Sources in Stand-Alone Systems

Chen M. X  Ho F. H  Cheng K. W. E

**Abstract−A simple and useful three-port converter is proposed in this paper, which is suitable for integrating renewable energy sources in off-grid applications with low to medium power. It mainly consists of a coupled inductor and two active switches. Isolation between the two renewable energy sources is achieved. Only one active switch functions in either loading mode or battery-charge mode. Hence the switching losses is reduced. Output diode of the proposed converter is removable from the system if one of the power source is integrated inside with anti-reversed-current diode, so that the system overall cost is reduced. Easy control techniques can be applied to the converter, since power decoupling control is not necessary due to out power constraint of a single PV panel. A 110*W* prototype was built and tested under loading mode and battery-charge mode to validate the theoretical analysis. Active snubber to eliminate voltage spike on the switches is introduced and results shown that zero-voltage switching (ZVS) is achieved.**

**Keywords−Three-port converter, less component count, simple control strategies**

## I. INTRODUCTION

Nowadays, due to the energy crisis and the side effects of burning fossil fuel, such as rapid growth of green-house gases (GHGs), global warming and rising sea level, it poses a threat to the existence of human beings. In order to deal with these problems, renewable energy sources (solar, wind, fuel cell) offer a good solution. Among these clean energies, solar is regarded as the most promising one. From satellite, electric vehicle (EV) to street lamp, the usage of photovoltaic or PV has fully penetrated the modern society [1]. Especially in stand-alone systems, it is very easy to harvest solar energy and transfer into electricity for off-grid applications (Fig. 1).

As it is known that the output voltage of a PV panel is variable and usually range from 20V to 40V (Fig. 2). Traditional way of using the solar energy in off-grid system is that a DC-DC converter is adopted to provide a constant output voltage which charges the battery. Thus, energy is captured and preserved for future usage when it is needed by discharging the battery. In this case, another DC-DC converter is also required to provide a regulated voltage for the load (motor, LED, etc) as shown in Fig. 3(a).

Recently, three-port converter (TPC) has become a popular topic in the application for renewable energies (Fig. 3(b)). It can provide an easy integration of multiple energy sources through a single converter, making energy transferred process more efficient compared with the traditional way of two-stage power transfer [2]. TPC with large DC gain are also discussed by many previous publications [3-5]. With high output voltage, they can provide suitable interfaces as the front-end to the renewable energy sources for on-grid applications [4]. However, power decoupling control is required where there is single-input-multiple-output (SIMO) operation mode [6]. Sometimes, additional active switches must be used to regulate the output voltages. However, not all applications require SIMO operation mode, such as in small electrical vessel systems or school shuttles. Due to the limited space, only one PV panel is allowed to be installed on the vessel. Other power sources such as battery is also included to ensure enough power for motor driving. Energy from solar panel is incapable to charge the battery and supplies the load at the same time. Under this constraint, available solutions for TPCs that containing SIMO (PV supplies output and charges battery simultaneously) is over design. Moreover, decoupling control for them is needed to regulate the output voltages, which will make the whole system more complex and less cost-effective.

In this paper, a simple TPC based on a coupled inductor is proposed to integrate the PV and battery in stand-alone system operating at medium power level (Fig. 4). Its features are as follows.

1) less component count: a coupled inductor, two active switches, one (or two) diode(s), two capacitors (including the output capacitor).
2) partly isolation: isolation between two power sources.
3) easy control and driving scheme: duty cycle control to regulate output voltage.
4) relatively high output voltage and low voltage stress.

The proposed TPC is cost-efficient because while components in the two-stage power converters have only one function, most components in the proposed TPC have multiple functions so that they can be shared in different modes, minimizing overall cost. Moreover, the relatively high output voltage reduces the number of the battery cells required in stand-alone systems. The proposed converter simplifies the power-transfer process compared with two-stage power conversion and increases the system efficiency. In the aforementioned-applications, (mostly in stand-alone systems with low to medium power rating) with input power constraint, without considering the decoupling control, simple control strategies can be applied. For easy understanding, the proposed converter is divided into two operation modes named as “loading mode” and “battery-charge mode”, and single PV panel and battery cells are considered as the renewable power sources.

In loading mode, the PV panel together with the battery supplies the load through the proposed TPC. Under extreme scenarios such as bad weather, the PV panel is by-passed by a diode and only the battery acts as the power source.

Battery-charge mode usually begins when the load is detached from the system (for example, the vessel stops).

**Power Electronics Research Centre, Department of Electrical Engineering, The Hong Kong Polytechnic University, Hong Kong**
**E-mail: mxchen@polyu.edu.hk**

The generated power from the PV is installed in the battery by charging it through the TPC. In this mode, switch $S_1$ is turned off, however, its body diode is still functioning to form a charge loop. If the charge current is large, it is recommended to place a diode $D_a$ in parallel with the body diode to reduce the conduction losses (Fig. 4 (b)).

The two operation modes of the proposed TPC are illustrated in detail below. The following assumptions are considered.

1) leakage inductance of coupled inductor is neglected, and turns ratio of the coupled inductor is $N_p : N_s = 1 : n$.
2) capacitors are large enough so that the voltages across them are treated as constant.
3) all the components are in ideal state. i.e. parasitic resistance is neglected.


(a) (b)

Fig. 1: PV application for small vessel. (a) Single PV panel consisting 72 cells (36V open circuit voltage). (b) Electrical vessel integrating with a PV panel and battery as power sources.

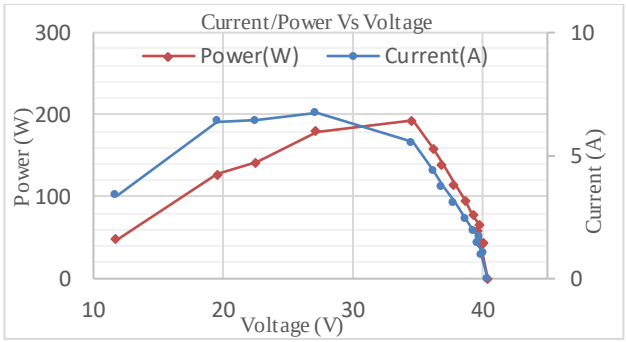
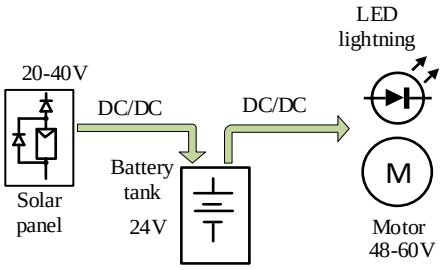
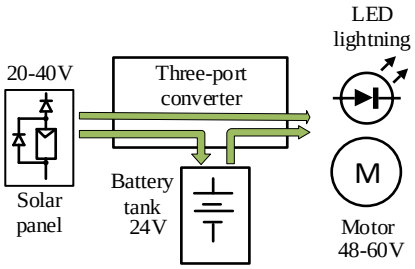



Fig.2: V/I characteristics and power output of a PV panel.




(a)




(b)

Fig. 3: Two ways of preserving and using the renewable energy. (a) Traditional way of two-stage energy conversion. (b) Another way of using three-port converter.

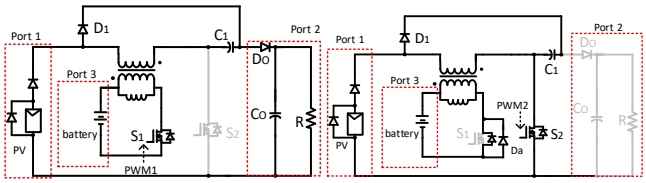



Fig. 4: Proposed TPC for off-grid application. (a) Loading mode. (b) Battery-charge mode

## II. Loading Mode Analysis of the Proposed TPC

In this mode, the load is connected to the converter. Both the PV and battery supply the load through a TPC. PV cannot charge the battery in this mode due to limited power. Switch $S_2$ is turned off at all time. Gating signal PWM1 drives $S_1$. The wingding connected in series with battery act as the primary side of the coupled inductor while the other wingding act as the secondary side. For easy understanding, leakage inductance of the coupled inductor is neglected. There are two switching stages for $S_1$ in this mode. Assume switching frequency of PWM1 driving signal is $f_s = \frac{1}{T}$, with duty cycle $D_1$. The two switching stages are illustrated in Fig. 5 (a, b).

Stage 1) switch on $(0 < t < D_1 T)$ (Fig. 5 (a)): during this stage, the main switch $S_1$ is turned on. Current from battery flowing through primary side of coupled inductor, main switch and then back to the battery. At the same time, the magnetizing inductor $L_m$ is getting charged by the battery voltage, with its current increases linearly.

$$i_{Lm} = \frac{V_{Lm}}{L_m} DT \quad (1)$$

$$V_{Lm} = V_b \quad (2)$$

where $V_{Lm}$ is the voltage across the primary side of coupled inductor. In the secondary side, current flowing out of PV panel, going through secondary side of coupled inductor, capacitor $C_1$ and then supplies the load. Energy stored in the capacitor $C_1$ discharges to the output, further stepping up the output voltage. Equations can be written

$$V_{pv} + V_s + V_{c1} = V_o \quad (3)$$

$$V_s = nV_{Lm} = nV_b \quad (4)$$

where $V_s$ is the voltage across the secondary side inductor.

This stage ends when the main switched is turned off and begins the next stage.

Stage 2) switch off ($D_1T < t < T$) (Fig. 5 (b)): in this stage, the main switch $S_1$ is turned off. Energy stored in the magnetizing inductor discharges to the secondary side through magnetic coupling. The output diode of PV panel is reversed biased, protecting PV from being damaged by the reversed current. Capacitor $C_1$ is getting charged by the voltage across the secondary side inductor. Output diode is reversed biased as well. And the output capacitor supplies the output, keeping a constant output voltage. Equations can be written in this stage

$$V_s = nV_{Lm} \quad (5)$$
$$V_s + V_{c1} = 0 \quad (6)$$

Of the two stages in loading mode, voltage-second balance is applied to the magnetizing inductor.

$$V_b D_1 T - \frac{V_{C1}}{n}(1 - D_1)T = 0 \quad (7)$$

By substituting equation (4) into (6), one can find the capacitor voltage $V_{c1}$ is

$$V_{c1} = \frac{nD_1}{1-D_1} V_b \quad (8)$$

And the DC gain of the TPC is

$$\mathrm{M} = \frac{n}{1-D_1} V_b + V_{pv} \quad (9)$$

Relatively high output voltage is obtained, which means the number of onboard battery cell can be reduced. And regulated output voltage is achieved by duty cycle control applied to PWM1.

The voltage stress on the switch $S_1$ and the diode $D_1$ are also found

$$V_{ds1} = \frac{1}{1-D_1} V_b \quad (18)$$
$$V_{d1} = \frac{n}{1-D_1} V_b \quad (19)$$

Low voltage stress on semiconductor devices which facilitate the use of switch with low on-resistor ($R_{ds\_on}$).

Average output current for the battery is calculated as follows.

$$\int_0^T I_b = \int_0^{DT} (I_p + I_{Lm}) dt \quad (10)$$

where $I_p$ is the average current flowing through primary side of coupled inductor and $I_{Lm}$ is the average magnetizing inductor current. They are represented as

$$\int_0^{DT} I_p \, dt = \int_0^{DT} nI_s \, dt = \int_0^{DT} nI_o \, dt \quad (11)$$
$$I_p = nI_o \quad (12)$$

Current-balance on capacitor $C_1$ yields

$$\int_{DT}^T I_{C1} = \int_0^{DT} I_o \quad (13)$$

where $I_{C1}$ is the average current of capacitor $C_1$ in switching stage stage 2. one can get

$$\int_{DT}^T I_{Lm} \, dt = \int_{DT}^T nI_{C1} \, dt \quad (14)$$
$$I_{Lm} = \frac{nD}{1-D} I_o \quad (15)$$

By substituting equations (12, 15) into (10), yields

$$I_b = \frac{n}{1-D} I_o \quad (16)$$

From Fig. 5 (a), one can get the average current for PV output is

$$I_{pv} = I_o \quad (17)$$

As the PV output diode and the converter output diode $D_o$ are both turned off at this stage, and they are in series connected in a loop. Voltage stress on the two diodes are

$$V_{do} = V_{dpv} = \frac{1}{2}(V_o - V_{pv}) = \frac{n}{2(1-D_1)} V_b \quad (20)$$

One may easily find that one of these two diodes is redundant and can be discarded. In practical cases, almost every PV panel is integrated inside with an output diode to prevent reversed current. So that the output diode $D_o$ is free to remove from the converter in applications where the overall system cost is a critical factor determining the converter design, provided that the voltage stress on output diode of PV panel isn't over the rated value. By doing so, the overall system cost is reduced, and the power conversion efficiency is expected to increase. Both two diodes are preserved in the above analysis and their voltage stress are halved compared with reduced-diode version. The key waveforms of the proposed TPC in loading mode is shown in Fig. 6.

It should be noted that there are two extreme scenarios in this mode. When sun irradiation is very low under bad weather, PV panel is bypassed by the bypass diode. The DC gain becomes

$$\mathrm{M} = \frac{n}{1-D_1} V_b \quad (21)$$

And higher duty cycle is applied to compensate for the loss of $V_{pv}$ (Fig. 7 (a)). When the battery is damaged or removed, PV may supply the load under some specific circumstances (Although it is not good to have the load running under rated power, it may be life-rescuing to drive the vessel back by using PV power source). In this case the TPC becomes a common DC converter whose output is

$$V_o = \frac{2-D_2}{1-D_2} V_{pv} \quad (22)$$

where $D_2$ is the duty cycle of switch $S_2$.

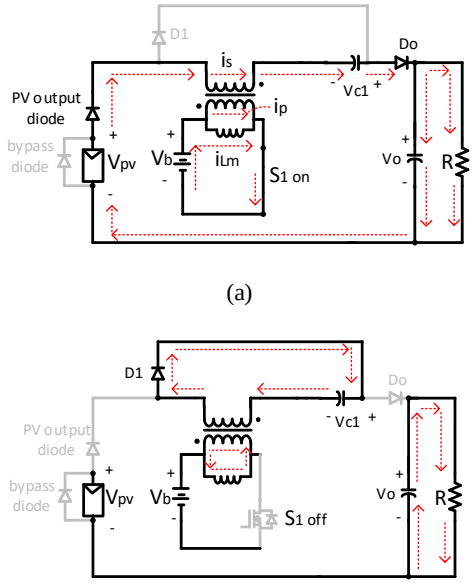



Fig. 5: Two switching stages of loading mode. (a) Switch $S_1$ on. (b) Switch $S_1$ off.

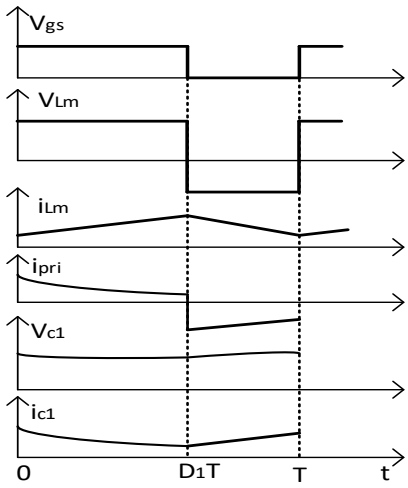



Fig. 6: Key waveforms of the proposed TPC in loading mode.

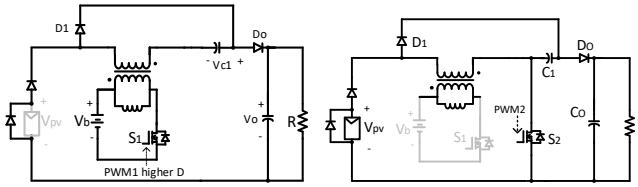



Fig.7: Two extreme scenarios in loading mode. (a) PV panel is bypassed. (b) Battery doesn't work.

## III. Battery-Charge Mode Analysis of The Proposed TPC

In this mode, the load is detached from the converter (Fig. 8 (a, b)). For an example, when the vessel stops running. Main switch $S_1$ is turned off all the time, while $S_2$ is turned on periodically. Body diode of $S_1$ still conducts in this mode. Additional diode can be placed in parallel to the body diode in high-power applications with high current. The wingding in series with PV acts as the primary side of the coupled inductor. The battery which stores the energy from PV panel is the load in this mode. Although diode $D_1$ remains, it is reversed biased all the time. Actually, the TPC becomes a fly-back converter in this mode. Results are given out here directly. The battery-charge voltage is regulated by the duty cycle $D_2$ of the driving signal PWM2.

$$V_b = \frac{n D_2}{1-D_2} V_{pv} \tag{23}$$

And the voltage stress on switch $S_2$ is

$$V_{ds2} = \frac{1}{1-D_2} V_{pv} \tag{24}$$

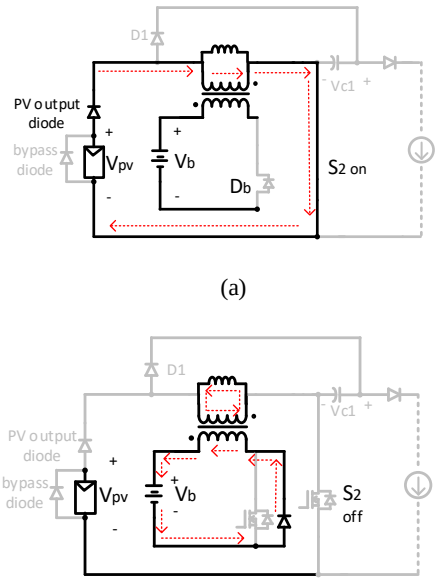



Fig. 8: Switching stages in battery-charge mode. (a) Switch on. (b) Switch off.

It should be noted that in this mode, energy generated by PV panel is used to charge battery only. The output cannot be supplied by the PV in this mode due to the lower power level. This is the difference between the proposed TPC and the available TPCs [1-6]. Instead, the converter changes to loading mode with double inputs when it is needed to supply the load.

## IV. Design Considerations

### *1. Coupled inductor design*

Consider that most of the PV output voltage $V_{pv}$ is in the range of 20-40V (30V nominal output), and the 24V battery cells are very common. Based on equation (15), the turns ratio of the coupled inductor is selected as $n = 1$.

In loading mode, apply current balance equation on capacitor $C_1$, one can find

$$I_o \times D_1 = I_{D1} \times (1 - D_1) \tag{25}$$

$$I_{D1} = I_{Lm} \tag{26}$$

where $I_{D1}$ and $I_{Lm}$ are the average current flowing through diode $D_1$ and the magnetizing inductor in Fig. 5 (b)

respectively. So the average current of magnetizing inductor can be expressed

$$I_{Lm} = \frac{D_1}{1-D_1} I_o \quad (27)$$

To ensure that the converter works at CCM and guarantee a good efficiency, 10% of current ripple for the magnetizing inductor is considered. Thus the magnetizing inductance should be calculated as

$$L_m = \frac{2V_b D_1 T}{10\%\ I_{Lm}} \quad (28)$$

Once the magnetic core is selected, the numbers of turns for primary and secondary side are found.

In battery-charge mode, similar method is used to find $L_m$. $L_m$ calculated in both modes are taken into consideration and the larger one is chosen for design.

*2. semiconductor component design.*
In loading mode, voltage stress for switch and diodes are found from equations (10-12).

The average current flowing through the switch S1 is

$$I_{ds} = I_{Lm} + I_p = \frac{1}{1-D_1} I_o \quad (29)$$

And its RMS value is

$$I_{ds\_rms} = I_{ds}\sqrt{D_1} \quad (30)$$

The average current flowing through output diode is $I_o$ (smaller values for the other average diode currents). Similar method is applied to batter charge mode and a comparative selection of the semiconductor components should be made.

## V. Simulation and Experimental Results

*1. Simulation Results*
The proposed converter is simulated by PSIM. Gating signal PWM1 is 100 kHz with 0.5 duty ratio. PV voltage is set to 30V and battery voltage is set to 24V in loading mode. Simulation results are shown in Figs. 9-10. Without adding voltage clamp circuit to the switch, a voltage spike is found in $V_{ds1}$ immediately after the switched turned off. The average output current of the PV is half of the battery's which matches with theoretical results in equation (16-17). In battery-charge mode, similar voltage spike is tested on the switch $S_2$. A constant output voltage is achieved to charge battery.

*2. Experimental Validation.*
To further examine the proposed converter, a prototype was built and tested. Configurations for the prototype are as follows.

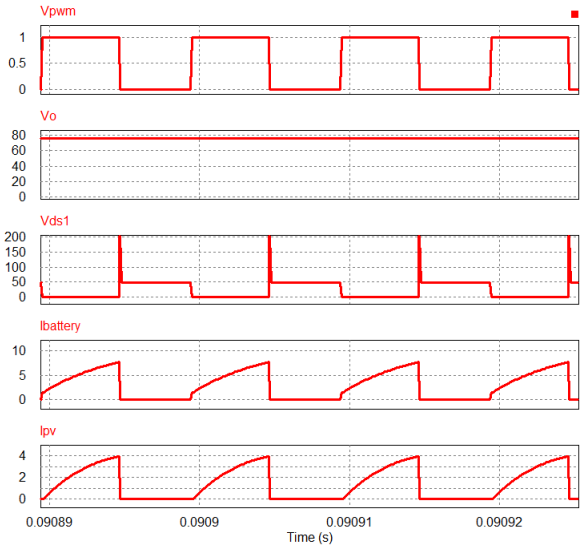



Fig. 9: Simulation results in loading mode with double inputs. Gating signal $V_{pwm}$; output voltage $V_o$; voltage stress on switch $S_1$, $V_{ds1}$; two input currents $I_{pv}$ and $I_{battary}$.

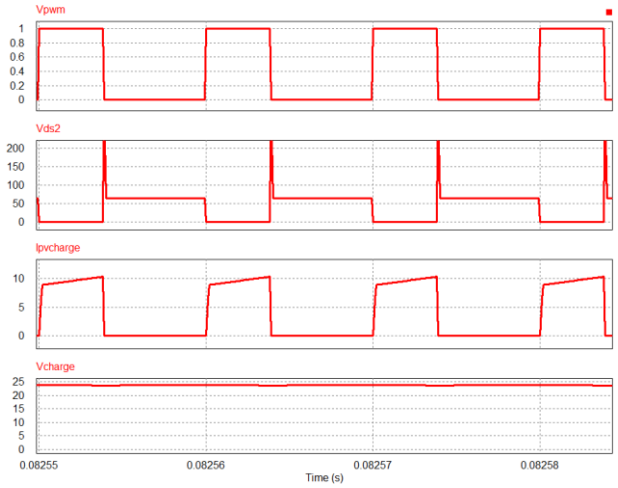



Fig. 10: Simulation results in battery-charge mode. gating signal $V_{pwm}$; battery-charge voltage $V_{charge}$; input currents $I_{pvcharge}$; voltage stress on switch $S_1$, $V_{ds1}$.

**Table I: Configurations for the Proposed Converter**

| | |
|---|---|
| Input voltage | $V_{pv} = 30V$, $V_b = 24V$ |
| Output voltage | $V_o = 68V, 100\ W$ |
| Switches $S_1, S_2$ | $FDPF51N25$ (250V,51A, $R_{ds_{on}} = 0.06\Omega$) |
| Diodes $D_1, D_o$ | $60EPU02PbF$ (200V, 60A) |
| Coupled inductor | $L_m = 122u, L_k = 1.3u.$ |
| Capacitors $C_1, C_o$ | 100V,200uF (ESR 0.05 Ω) |

The experimental results are shown in Figs. 11-12. Similar to the simulation results, voltage spike on switch is. It may also bring larger voltage ripple to the output in batter-charge mode.

*3. Improved Performances test*
To improve the converter performances, two active snubbers are added at the primary and secondary sides of the coupled inductor to eliminate voltage spike on the switches. L-C filter to minimize the output current ripple of PV panel is also added. Zero-voltage switching (ZVS) is achieved by the switches.

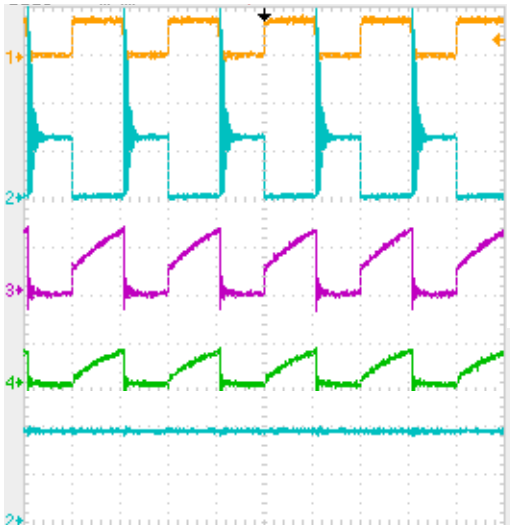


Fig. 11: Experimental results in loading mode with double inputs. Gating signal $V_{pwm}$; output voltage $V_o$ $(40V/div)$; voltage stress on switch $S_1$ , $V_{ds1}$ $(40V/div)$; two input currents $I_{pv}$ $(5A/div)$ and $I_{battary}$ $(5A/div)$.

Fig. 12: Experimental results in battery-charge mode. gating signal $V_{pwm}$; battery-charge voltage $V_{charge}$ $(10V/div)$; input currents $I_{pvcharge}$ $(5A/div)$; voltage stress on switch $S_1$, $V_{ds1}$ $(40V/div)$.

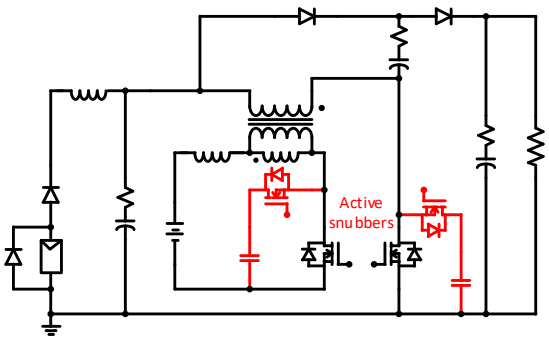



Fig. 13: Including active snubber to clamp voltage on switch.

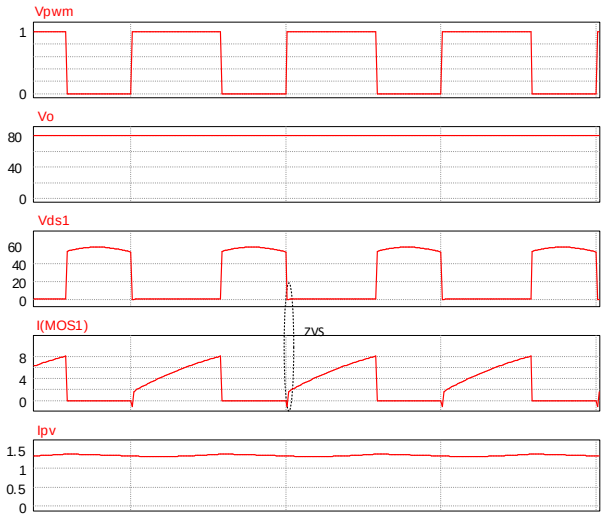



Fig. 14: Simulation results in loading mode with double inputs. Gating signal $V_{pwm}$; output voltage $V_o$; voltage stress on switch $S_1$, $V_{ds1}$; two input currents $I_{pv}$ and $I_{battary}$.

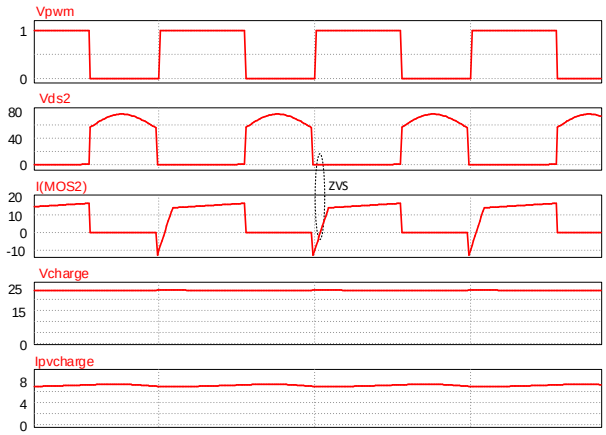



Fig. 15: Simulation results in battery-charge mode. gating signal $V_{pwm}$; battery-charge voltage $V_{charge}$; input currents $I_{pvcharge}$; voltage stress on switch $S_1$, $V_{ds1}$.

## VI. Conclusions and Future Discussions

A very simple and useful three-port converter (TPC) is proposed. The proposed converter uses less power devices such as Mosfet or diode but provides an easy integration for multiple renewable energies sources. In loading mode and batter-charge mode, the output voltage is regulated by duty cycle of the switch signals $D_1$ and $D_2$, no complex control required. The converter with active clamp circuit to deal with the leakage inductance is simulated and results show that ZVS is achieved. Yet, the cost of the system is increased. So a trade-off between converter cost and the power transfer efficiency exists when designing the proposed TPC.

## References

[1] J. P. Benner and L. Kazmerski, “Photovoltaics gaining greater visibility,” IEEE Spectr., vol. 29, no. 9, pp. 34–42, Sep. 1999.

[2] N. Zhang, D. Sutanto, K. M. Muttaqi, “A review of topologies of three-port DC–DC converters for the integration of renewable energy and energy storage system,” *Renewable and Sustainable Energy Reviews*, 56 (2016) 388–401.

[3] Y. Chen, A. Q. Huang and X. Yu, “A High Step-Up Three-Port

DC–DC Converter for Stand-Alone PV/Battery Power Systems," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5049-5062, Nov. 2013.

[4] L. Chien, C. Chen, J. Chen and Y. Hsieh, "Novel Three-Port Converter with High-Voltage Gain," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4693-4703, Sept. 2014.

[5] H. Wu, K. Sun, R. Chen, H. Hu, and Y. Xing, "Full-Bridge Three-Port Converters with Wide Input Voltage Range for Renewable Power Systems," *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 3965-3974, Sept. 2012.

[6] C. Zhao, S. Round and J. Kolar, "An Isolated Three-Port Bidirectional DC-DC Converter with Decoupled Power Flow Management," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2443-2453, Sept. 2008.

# Experimental Study on the Electrical Characteristic of a GaN Hybrid Drain-embedded Gate Injection Transistor (HD-GIT)

Fong Y. C[1] Cheng K. W. E[2]

**Abstract–The hybrid drain-embedded gate injection transistor (HD-GIT) is a well-developed structure of GaN-based power transistor which solves the issues of current collapse and negative gate threshold voltage. In this paper, the electrical characteristic of a HD-GIT-based GaN power transistor is investigated with experimental study. Based on the gate I-V relationship, the design of the gate driver circuit is discussed. The gate driving losses as well as the switching waveforms of the HD-GIT under hard-switching operations are analyzed. Besides speeding up the switching operation, the reduction in the gate voltage and gate charge saves the gate driving power. These features substantially increase the maximum operating frequency of the HD-GIT-based power converter. The current collapse free operation allows the device working at a wide range of voltage and duty cycle without notable degradation of the dynamic on-state resistance.**

**Keywords–Gallium Nitride (GaN), high-electron-mobility transistor (HEMT).**

## I. Introduction

Semiconductor switches are the key elements of power electronic converters. At present, these power semiconductor devices in the industry are mainly based on the mature Si technology. However, the increasing requirements of high-frequency and high-voltage capabilities of these devices are reaching the physical limits of the Si technology. In order to get rid of the bottleneck in the performance of switching devices, the semiconductor industries have started seeking for alternative power semiconductor materials in recent years. The wide bandgap (WBG) semiconductor materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) exhibit many superior features over the conventional counterparts. These features include: high blocking voltage, high electron velocity as well as high-temperature capability [1-3], which make these WBG semiconductor materials highly potential for the future power devices.

The GaN-based high electron mobility transistors (HEMTs) have demonstrated remarkable improvements on the power density and efficiency for high frequency power applications such as radiofrequency (RF) and microwave amplifiers. [4-8] In recent years, the adoption of GaN transistors in power converter applications has been reported and confirmed the potential in small footprint and efficient DC-DC converters with conventional hard-switched topologies [9-10]; bidirectional converters for energy storage systems in DC microgrids [11]; integrated converters for vehicular applications [12]; as well as single-phase AC inverters for low-frequency power supply [13] and high-frequency wireless power transfer [14].

**Power Electronics Research Centre, Department of Electrical Engineering, The Hong Kong Polytechnic University, Hong Kong**
**E-mail: yc-chi.fong@connect.polyu.hk**

Along with the GaN technology maturation, the GaN switches show prominent competitive power in the market. For example, the development of GaN-on-Si fabrication techniques [15-19] has noticeably reduced the material cost; the cascode structure [20] and the gate injection technology [16] offer the normally off options which make them more ready for direct substitution of the Si counterparts. Engineering samples of GaN power transistors are currently available in the market for research and development purposes. In this paper, the experimental study of the GaN power transistor sample with the latest hybrid drain-embedded gate injection transistor (HD-GIT) structure [21] is presented. The electrical characteristic of the HD-GIT sample was measured and modeled. Also, the design considerations such as the gate driver circuit and the switching loss analysis are discussed.

## II. Review on the HD-GIT Technology

The HD-GIT structure [21-24] is an improved version of HEMT which also utilizes 2D electron gas with high electron mobility formed at the interface between GaN and AlGaN for conduction; but the gate threshold voltage is altered for normally-off operation [17], [24] and the current-collapse issue is eliminated [22-23].

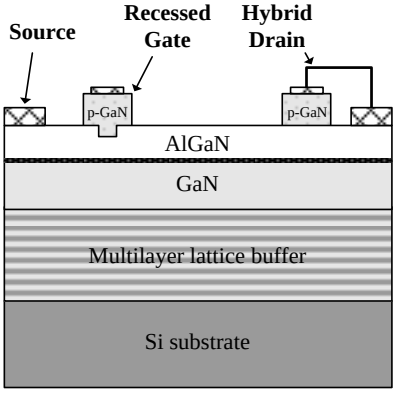



Fig. 1: Simplified schematic cross section diagram of the HD-GIT structure [21-23]

The simplified schematic cross section of the HD-GIT structure is illustrated in Fig. 1 [21-23]. The holes injected from the p-doped recessed gate significantly increase the threshold voltage of the transistor and make the GIT normally-off. When voltage is applied across the gate and the source which is exceeding the GIT's threshold voltage, the hole is injected to the channel and the electrons can flow with high mobility. Since the hole mobility is significantly lower than that of electrons, the gate current is kept at low level, in the order of mill-amperes. Besides, the supplementary p-GaN region adjacent to the drain electrode suppresses the current-collapse issue by injecting

holes which recombine with the trapped electrons near the channel [22-23].

For the consideration of material cost effectiveness, the GIT is grown on silicon substrate; the lattice and thermal mismatches [17], as well as the wetting issues [15] are avoided by insertion of the multilayer lattice buffer [21]. The designs in [17] and [22] suggest that the buffer could be formed by AlGaN/AlN and GaN/AlN layers.

## III. Specification of the HD-GIT Sample

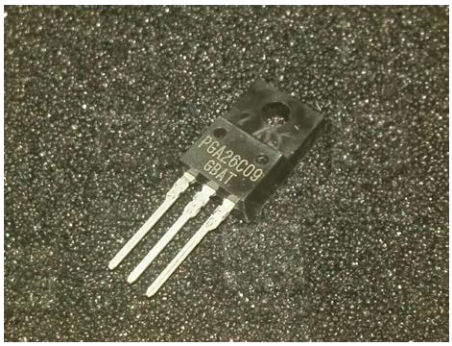



Fig. 2: The PGA26C09DV [25] HD-GIT sample in TO-220D package

**Table 1: Specification of the HD-GIT sample [25]**

| Item | Value |
|---|---|
| Package | TO-220D |
| $V_{ds(max)}$ | 600V |
| $I_{d(max)}$@$T_c$ = 25℃ | 15A |
| $R_{ds(on)}$ @$I_{gs}$ = 21.4mA and $T_j$ = 25℃ | 71mΩ |
| $V_{gs}$ | -10V to 4.5V |
| $V_{gs(th)}$ | 1.2V |
| $r_g$ | 4.4Ω |
| $Q_g$ @$V_d$ = 400V and $I_{ds}$ = 8A | 6nC |

In this work, the PGA26C09DV [25] X-GaN power transistor in TO-220D package (Fig. 2), was used to study the electrical characteristic of HD-GIT structure-based GaN power transistor. The voltage and current ratings are 600V and 15A, respectively. Referring to the preliminary datasheet [25] provided by the supplier, the basic specifications of the HD-GIT are listed in table 1.

## IV. Electrical Characteristic of the HD-GIT

The HD-GIT has different gate characteristic comparing to ordinary MOSFETs. Continuous gate current at mill-amperes is required to keep the device at on state. The $I_{gs}$-$V_{gs}$ characteristic can be simulated as a diode connecting between the gate and the source terminals. A simplified electrical model of a GaN HEMT is depicted in Fig. 3 [26-27]. At steady-state, the gate terminal is equivalent to a diode with series resistance. The drain is represented by a current source with gate voltage dependent transconductance $g_m$ and series resistances connecting to the source terminal.

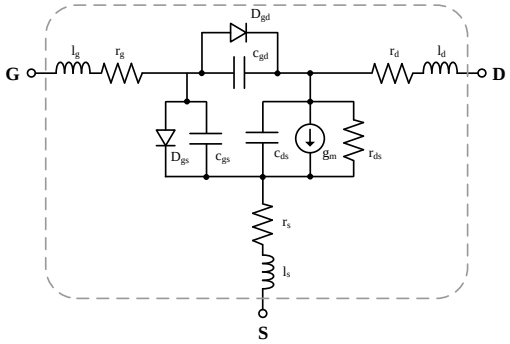



Fig. 3: Simplified electrical model of the GaN HEMT [26-27]

In order to examine the electrical characteristic of the device at steady-state, as well as during switching operation, the experimental setups with respective measuring circuits were implemented.

### *1. Gate Characteristic*

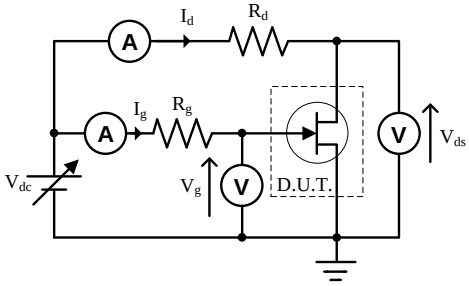



Fig. 4: The schematic of the experimental setup for measuring the steady-state gate characteristics of the HD-GIT

The measurement setup for steady-state gate characteristic is shown in Fig. 4. The external gate resistor, $R_g$, and drain resistor, $R_d$, were 1kΩ and 250Ω, respectively. By varying the voltage source, $V_{dc}$, the $I_{gs}$-$V_{gs}$ curve and the corresponding steady-state drain-to-source resistance were measured.

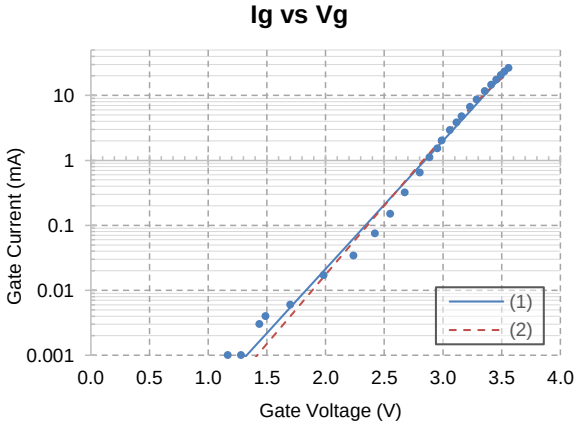
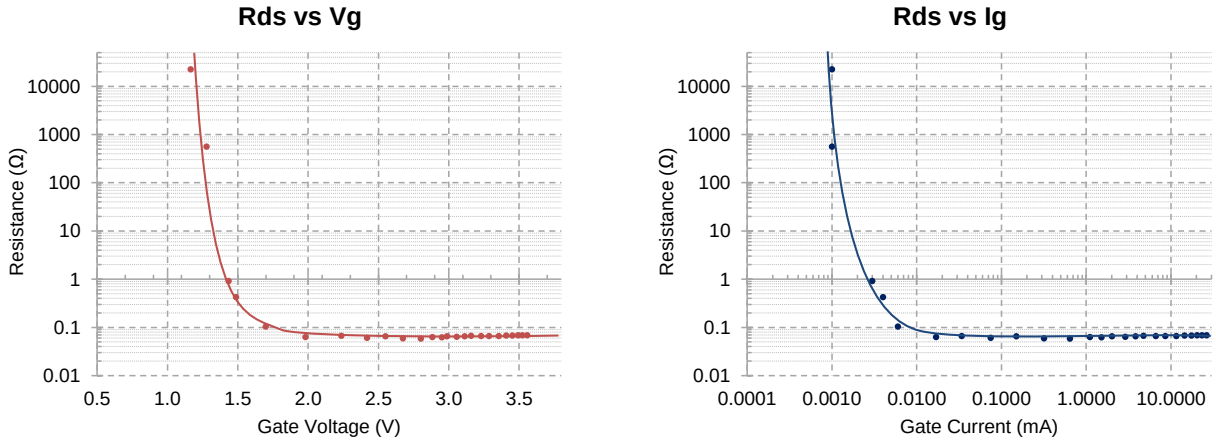



Fig. 5: The measured gate current to gate voltage ($I_{gs}$-$V_{gs}$) characteristic of the HD-GIT and the fitted curves ($T_a$ = 23℃)

The gate current to gate voltage ($I_{gs}$-$V_{gs}$) curve is plotted in Fig. 5. By directly fitting the measured data with the well-known diode equation, the gate current could be approximated by the following function.




(a) (b)

Fig. 6: Measured drain-to-source resistance $R_{ds}$ of the HD-GIT sample ($T_a$ = 23°C); (a) $R_{ds}$ to the gate voltage, $V_{gs}$; (b) $R_{ds}$ to the gate current, $I_{gs}$

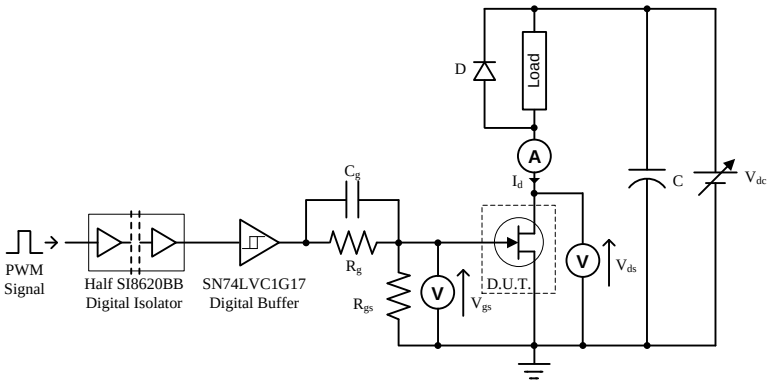



Fig. 7: The testing circuit, comprising an isolated gate driver and a loading circuit, for the low side HD-GIT

$$I_g = 2.4e-9\left(e^{\frac{V_{gs}}{0.22}}-1\right) \quad (1)$$

If the listed gate resistance, $r_g$ = *4.4Ω*, is used to adjust the measured gate voltage, the fitted equation becomes

$$I_g = 9.6e-10\left(e^{\frac{V_{gs}-4.4I_g}{0.204}}-1\right) \quad (2)$$

As shown in Fig. 5, it could be observed that the difference between the fitted curves, (1) and (2), is insignificant. In most cases, the simplified curve (1) would be accurate enough for the calculation of external gate resistor value, $R_g$ in power switching applications.

At the same time, the on-state drain-to-source resistance, $R_{ds}$, was measured with $V_{ds}$ and $I_{ds}$. The responses of $R_{ds}$ to the gate voltage and current are plotted in Fig. 6. The measured curve in Fig. 6(a) was similar to the $R_{ds}$ to gate voltage curves of logic level MOSFETs. The $R_{ds}$ of the HD-GIT dramatically dropped at the gate threshold voltage of around 1.2V and cropped at about 65mΩ. However, unlike the MOSFETs, the HD-GIT requires continuous gate current to hold the device at on state (Fig. 6(b)). At gate plateau voltage of around 1.5V, the gate current was about 5μA.

*2. Gate Driver Circuit*

Based on the measured gate characteristic of the HD-GIT in previous section, the drain-to-source resistance of the device reaches stable value at around $V_{gs}$ = 3V and $I_{gs}$ = 2mA. By adding a margin of 0.3V to 0.5V and substitute the gate-to-source voltage values into (1), the steady-state gate current, $I_{g(on)}$ would be about 7.84mA to 19.47mA. Considering that the gate driving losses are determined by the operating voltage of the gate driver; instead of ordinary gate driver of 10V to 15V operating voltage, a Schmitt-trigger buffer, SN74LVC1G17, which operates at 5V, was employed. The external gate resistance, $R_g$, was selected according to (3),

$$R_g = \frac{V_{OH} - V_{gs(on)}}{I_{g(on)}} \quad (3)$$

where $V_{OH}$ is the high-level output voltage of the digital buffer.

In order to speed up the on and off transients, a series connected capacitance, $C_g$, was added between the buffer's output and the gate terminals for providing inrush current to charge up the intrinsic capacitance quickly; and also providing negative voltage to ensure off state of the device during low output logic level of the buffer. The selection of $C_g$ follows equation (4) [28].

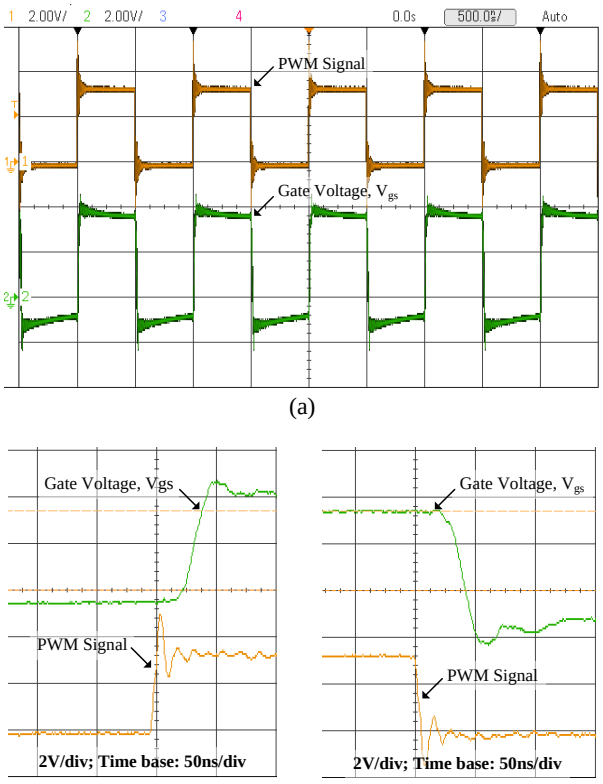



Fig. 8: The measured gate waveforms at 1MHz and 50% duty cycle; (a) the PWM signal and the corresponding gate voltage; (b) zoomed in waveforms at ON transient; (c) zoomed in waveforms at OFF transient

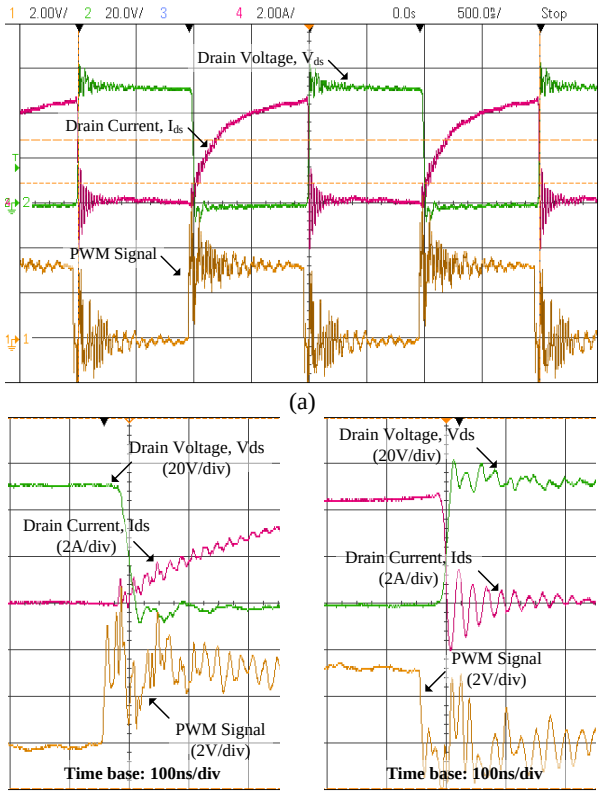



Fig. 9: The measured output waveforms at 500kHz and 50% duty cycle; (a) the PWM signal and the corresponding drain voltage and current; (b) zoomed in waveforms at ON transient; (c) zoomed in waveforms at OFF transient

$$C_g = \frac{Q_g}{V_{OH} - V_{gs(on)} - V_{neg}} \tag{4}$$

In addition, an external parallel resistor, $R_{gs}$, with high resistance was inserted between the gate and source terminals of the device to pull the gate voltage down and ensure the device is in off state when the gate driver circuit is not powered. Based on the listed values in the datasheet of the HD-GIT and on-state voltage margin of 0.3V to 0.5V and negative voltage of 1V, the calculated $R_g$ and $C_g$ were 77.0Ω to 216.8Ω and 10.9nF, respectively.

In the testing circuit, external gate resistance of $R_g$ = 100Ω, and series capacitor of $C_g$ = 10nF were selected. Moreover, a low-power digital isolator, SI8620BB, was employed to provide galvanic isolation between the signal and power circuits. The gate driving waveforms at 1MHz, generated by the testing circuit, are shown in Fig. 8. The propagation delay time was around 32ns, while the rise and fall time were around 14ns for both turning on and off.

*3. Hard-switching Performance*

A voltage source of $V_{dc}$ = 50V and an inductive load of about 10Ω were employed in the testing circuit. The HD-GIT was switched at 500kHz. The drain-to-source voltage and the drain current waveforms of the device under hard-switching operation were measured (Fig. 9). As illustrated in the switching waveforms, the durations for the HD-GIT to turn on and off under loading were approximately 20ns and 12ns, respectively. In general, shorter durations for turning on and off would cause lesser switching losses in hard-switched power converters.

### 3.1. Gate driving Loss Analysis

The gate driving losses for the HD-GIT consist of two major parts – 1) the charge-up losses of the device's intrinsic capacitance, and 2) the conductance losses caused by continuous gate current during on-state. Therefore, the gate driving losses, $P_{drive}$, would be approximately

$$P_{drive} = V_{OH}\left(DI_{g(on)} + fQ_g\right) \tag{5}$$

where D is the duty cycle and *f* is the switching frequency of the device. Although the HD-GIT requires continuous gate current at on state, the reduction in the driving voltage and gate charge could significantly reduce the gate driving losses at high frequency operation.

### 3.2. Switching Loss Analysis

The magnitude of the energy losses during the ON and OFF operations of the switches are highly dependent on the switching duration, $T_{sw}$, which the voltage and current waveforms of the switch are overlapping each other. The switching energy losses, $E_{sw}$, can be evaluated as (6).

$$E_{sw} = \int_0^{T_{sw}} V_{ds}(t)\, I_{ds}(t)\, dt \tag{6}$$

which can be estimated by linear approximation and simplified to

$$E_{sw} = \frac{V_{ds(off)} I_{ds(on)} T_{sw}}{6} \tag{7}$$

where $V_{ds(off)}$ is the drain-to-source voltage across the transistor before the on transition or after the off transition while $I_{ds(on)}$ is the drain current of the transistor before the off transition or after the on transition. Hence, the switching power losses, $P_{sw(loss)}$, of the semiconductor switches are directly proportional to the operation frequency and the duration of the switching operations.

$$P_{sw(loss)} = \frac{fT_{sw}V_{ds(off)}I_{ds(on)}}{3} \quad (8)$$

Considering the product, $V_{ds(off)}I_{ds(on)}$, is the order of power handling of the semiconductor switches, in order to keep the switching losses below the target factor, α, the maximum operation frequency, $f_{max}$, of the hard switching semiconductor switch should be

$$f_{\max} = \frac{3\alpha}{T_{sw}} \quad (9)$$

For example, if the target switching losses factor is 1%; and the WBG switch having average hard switching duration of 20ns, the maximum operation frequency would be

$$f_{\max} = \frac{3\times 0.01}{20e-9} = 1.5MHz \quad (10)$$

*5. Study on the Current Collapse Issue*

Current collapse due to trapping effects is characterized in conventional AlGaN/GaN HEMTs that the $R_{ds(on)}$ increases dramatically after applying voltage stress across the drain and source terminals of the device [29]. The degradation of dynamic on-state resistance [30] at high operating voltage would pose a challenge to power electronics design engineers. The HD-GIT structure employed in the sample device of this study was featured as current collapse free [25] at the rated voltage. This feature has been demonstrated in [22] and [23] by applying high voltage pulses with fixed duty cycle to analyze the saturated dynamic $R_{ds(on)}$.

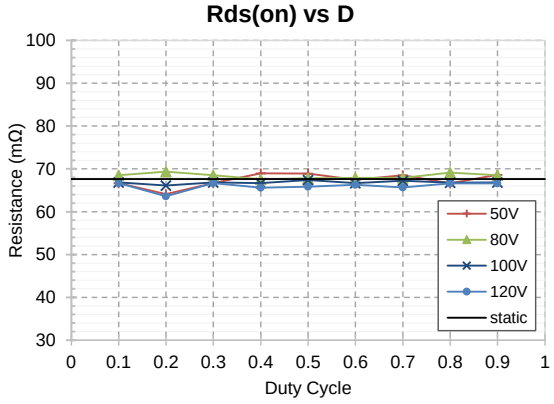



Fig. 10: The measured on-state resistance of the HD-GiT sample under different duty cycle, D, and applied voltage

As the trapping effects is a time-accumulative phenomenon [29-30], duty cycle was used as the variable to demonstrate the equilibrium $R_{ds(on)}$. As illustrated in Fig. 10, no distinct relationship between the on-state resistance and duty cycle could be observed, which suggests that the effects of the dynamic $R_{ds(on)}$ of this HD-GIT would be negligible in practical application.

## V. SUMMARY

The WBG semiconductor devices have exhibited their superiority features over the conventional Si technology. The HD-GIT is one of the most well developed structures for GaN power transistors which overcome many practical issues such as the unstable and negative gate threshold voltage and the current collapse phenomenon. Comparing with Si-based MOSFETs and IGBTs, the GaN HEMTs have quite different electrical characteristics; therefore, the gate driver design, hard-switching feature as well as the dynamic on-state resistance should be taken into consideration in the substitution of Si-based devices. This paper demonstrates the gate and switching characteristics of a HD-GIT in circuit design point of view. Due to the reduction in the gate charge and required gate voltage, the gate driving losses at high frequency operation could be greatly reduced compared to the Si-based MOSFETs and IGBTs. The substantial increase in switching speed and the current collapse free operation allow hard-switched power converter design at high power density.

## ACKNOWLEDGMENT

The authors wish to thanks Dr. In-suk Choi for the discussion on the lattice structures and material science of semiconductor devices. The research is support by Power Electronics Research Centre (PERC) and Research Committee at The Hong Kong Polytechnic University.

## REFERENCES

[1] P. G. Neudeck, R. S. Okojie and L. Y. Chen, "High-temperature electronics - a role for wide bandgap semiconductors?," in *Proc. of the IEEE*, vol. 90, no. 6, pp. 1065-1076, Jun 2002.

[2] M. A. Khan, G. Simin, S. G. Pytel, A. Monti, E. Santi and J. L. Hudgins, "New Developments in Gallium Nitride and the Impact on Power Electronics," *2005 IEEE 36th Power Electron. Specialists Conf.*, Recife, 2005, pp. 15-26.

[3] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in *IEEE Trans. on Power Electron.*, vol. 29, no. 5, pp. 2155-2163, May 2014.

[4] S. T. Sheppard, K. Doverspike, W. L. Pribble, S. T. Allen, and J.W. Palmour, "High power microwave GaN/AlGaN HEMTs on siliconcarbide," in *IEEE Electron Device Lett.*, vol. 20, pp. 161–163, Apr. 1999.

[5] Y. F.Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, and U. K. Mishra, "Very-high power density AlGaN/GaN HEMTs," in *IEEE Trans. Electron Devices*, vol. 48, pp. 586–590, Mar. 2001.

[6] L. Shen *et al.*, "AlGaN/AlN/GaN high-power microwave HEMT," in *IEEE Electron Device Letters*, vol. 22, no. 10, pp. 457-459, Oct. 2001.

[7] J. W. Johnson *et al.*, "12 W/mm AlGaN-GaN HFETs on silicon substrates," in *IEEE Electron Device Letters*, vol. 25, no. 7, pp. 459-461, July 2004.

[8] U. K. Mishra, L. Shen, T. E. Kazior and Y. F. Wu, "GaN-Based RF Power Devices and Amplifiers," in *Proc. of the IEEE*, vol. 96, no. 2, pp. 287-305, Feb. 2008.

[9] Y. Wu, M. Jacob-Mitos, M. L. Moore and S. Heikman, "A 97.8% Efficient GaN HEMT Boost Converter With 300-W Output Power at 1 MHz," in *IEEE Electron Device Letters*, vol. 29, no. 8, pp. 824-826, Aug. 2008.
[10] R. Ramachandran and M. Nymand, "Experimental Demonstration of a 98.8% Efficient Isolated DC–DC GaN Converter," in *IEEE Trans. on Ind. Electron.*, vol. 64, no. 11, pp. 9104-9113, Nov. 2017.
[11] F. Xue, R. Yu and A. Q. Huang, "A 98.3% Efficient GaN Isolated Bidirectional DC–DC Converter for DC Microgrid Energy Storage System Applications," in *IEEE Trans. on Ind. Electron.*, vol. 64, no. 11, pp. 9094-9103, Nov. 2017.
[12] P. Choi, U. Radhakrishna, C. C. Boon, D. Antoniadis and L. S. Peh, "A Fully Integrated Inductor-Based GaN Boost Converter With Self-Generated Switching Signal for Vehicular Applications," in *IEEE Trans. on Power Electron.*, vol. 31, no. 8, pp. 5365-5368, Aug. 2016.
[13] C. Zhao *et al*., "Design and Implementation of a GaN-Based, 100-kHz, 102-W/in$^3$ Single-Phase Inverter," in *IEEE Journal of Emerging and Selected Topics in Power Electron.*, vol. 4, no. 3, pp. 824-840, Sept. 2016.
[14] C. Zhao and D. Costinett, "GaN-Based Dual-Mode Wireless Power Transfer Using Multifrequency Programmed Pulse Width Modulation," in *IEEE Trans. on Ind. Electron.*, vol. 64, no. 11, pp. 9165-9176, Nov. 2017.
[15] P. Chen, R. Zhang, Z.M. Zhao, D.J. Xi, B. Shen, Z.Z. Chen, Y.G. Zhou, S.Y. Xie, W.F. Lu, Y.D. Zheng, "Growth of high quality GaN layers with AlN buffer on Si(111) substrates," in *Journal of Crystal Growth*, vol. 225, no. 2–4, pp. 150-154, 2001.
[16] K. Y. Zang, S. J. Chua, L. S. Wang, C. V. Thompson, "Evolution of AlN buffer layers on silicon and effects on the properties of epitaxial GaN films," in *phys. stat. sol.*, 0: 2067–2071, 2003.
[17] Y. Uemoto *et al*., "Gate Injection Transistor (GIT)—A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation," in *IEEE Trans. on Electron Devices*, vol. 54, no. 12, pp. 3393-3399, Dec. 2007.
[18] N. Ikeda, S. Kaya, J. Li, T. Kokawa, Y. Satoh and S. Katoh, "High-power AlGaN/GaN HFETs on Si substrates," *The 2010 Int. Power Electron. Conf. - ECCE ASIA -*, Sapporo, 2010, pp. 1018-1022.
[19] W. Mateusz, P. Bogdan, S. Tomasz, P. Regina, "Optimization of AlGaN/GaN/Si(111) buffer growth conditions for nitride based HEMTs on silicon substrates," in *Journal of Crystal Growth*, vol. 414, pp. 248-253, 2015.
[20] X. Huang, Z. Liu, Q. Li and F. C. Lee, "Evaluation and Application of 600 V GaN HEMT in Cascode Structure," in *IEEE Trans. on Power Electron.*, vol. 29, no. 5, pp. 2453-2461, May 2014.
[21] (2017). [Online]. Available: eu.industrial.panasonic.com/products/semiconductors/power/gan-power-transistors
[22] K. Tanaka *et al.*, "Suppression of current collapse by hole injection from drain in a normally-off GaN-based hybrid-drain-embedded gate injection transistor," in *Appl. Physics Letters*. vol.107, 163502, Oct. 2015.
[23] S. Kaneko *et al*., "Current-collapse-free operations up to 850 V by GaN-GIT utilizing hole injection from drain," *2015 IEEE 27th Int Symp. on Power Semicond. Devices & IC's (ISPSD)*, Hong Kong, 2015, pp. 41-44.
[24] H. Okita *et al*., "Through Recess and Regrowth Gate Technology for Realizing Process Stability of GaN-Based Gate Injection Transistors," in *IEEE Trans. on Electron Devices*, vol. 64, no. 3, pp. 1026-1031, Mar. 2017.
[25] Preliminary Datasheet PGA26C09DV, 2015 [Online]. Available: mouser.com/pdfdocs/PreliminaryTO220GANDatasheetPGA26C09DV.pdf
[26] S. Aamir Ahsan, S. Ghosh, S. Khandelwal and Y. S. Chauhan, "Physics-Based Multi-Bias RF Large-Signal GaN HEMT Modeling and Parameter Extraction Flow," in *IEEE Journal of the Electron Devices Society*, vol. 5, no. 5, pp. 310-319, Sept. 2017.
[27] Y. Xu *et al*., "A Scalable Large-Signal Multiharmonic Model of AlGaN/GaN HEMTs and Its Application in C-Band High Power Amplifier MMIC," in *IEEE Trans. on Microwave Theory and Techniques*, vol. 65, no. 8, pp. 2836-2846, Aug. 2017.
[28] E. Gurpinar and A. Castellazzi, "Single-Phase T-Type Inverter Performance Benchmark Using Si IGBTs, SiC MOSFETs, and GaN HEMTs," in *IEEE Trans. on Power Electron.*, vol. 31, no. 10, pp. 7148-7160, Oct. 2016.
[29] M. Meneghini *et al*., "Time- and Field-Dependent Trapping in GaN-Based Enhancement-Mode Transistors With p-Gate," in *IEEE Electron Device Letters*, vol. 33, no. 3, pp. 375-377, March 2012.
[30] N. Badawi, O. Hilt, E. Bahat-Treidel, J. Böcker, J. Würfl and S. Dieckerhoff, "Investigation of the Dynamic On-State Resistance of 600 V Normally-Off and Normally-On GaN HEMTs," in *IEEE Trans. on Ind. Appl.*, vol. 52, no. 6, pp. 4955-4964, Nov.-Dec. 2016.

# Human Impedance Characteristic Investigation by Low Voltage Square Wave Excitation

Xu C. D[1] Cheng K. W. E[2] Wang D. H[3]

**Abstract–In order to obtain the characteristic of the human impedance [1][2], A square wave electric signal is proposed to apply to the human beings. The peak current when a human is in initial contact of an electrical signal is examined. The use of square wave is a better method for human detection as it gives an exponential current that is unique as compared to another electrical appliance. The result provides a critical judgment for smart electric socket which could identify human being from another appliance.**
**The whole research is based on the human model in the standard of IEC 479[3]. Considering the instant effect in the first charging moment by the step pulse, the human model is simplified to an RC circuit.**

**Keywords–Human impedance, square wave excitation, safety**

## I. INTRODUCTION

Traditional safety product cannot identify the human body from the other electric load because of the overtime and complication of the human body impedance data [4]. To reduce the human body risk against the shock and touch current, the human body impedance test is carried on providing the updated data based on the international standard human impedance model in standard of IEC 479.

As shown in Fig. 1. The human impedance consists of skin resistor $R_1$ and $R_2$ paralleled with capacitor $C_1$ and $C_2$ connected with internal resistor.

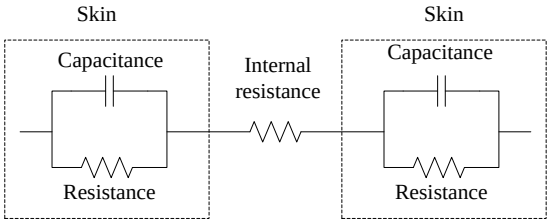



Fig. 1: The model of human body

As mentioned in the standard, the skin resistance $R_1$ and $R_2$ are around several hundred k ohm, the internal resistance is around 500-1000 ohm. From the experimental results, the skin capacitance $C_1$, $C_2$ are few pF.

In the proposed method, the human impedance is obtained by applying a square wave low voltage power source to the human body. For square waveform [5], the rise time of square waveform is very fast and is about 100-200ns in ESIC circuit. When the human capacitance starts being charged, there is current flowing through the whole body. The value of R1 and R2 is several hundred k ohm from IEC 479, the current flowing through $R_1$ and $R_2$ is very small that is about 60 uA for square waveform of 24V and $R_1$ and $R_2$ assumed to be 200k ohm. Meanwhile, the peak current flowing human is generally higher than 10mA from experiment data. The current flowing through $R_1$ and $R_2$ is 0.6% of peak current, that is, most current flows through $C_1$, $R_0$ and $C_2$. Therefore, the human model could be simplified into a RC model at the step pulse moment as shown in Fig. 2.


Fig. 2: Simplified RC model

From the up and down edge of the wave, the internal resistor and the charging time could be obtained. In order to identify human body from other electric load, analysis and conclusion is made. Human body could be identified by the peak current and the pulse time.

From the experiments result, human impedance is very stable with a fixed internal resistor connected with a changing capacitor.

## II. TEST APPARATUS AND TEST PROCEDURE

The equipment like Signal Generator (AFG3021B), Power Amplifier, Digital Storage Oscilloscope (DSO-X 3024A), AC/DC Current Probe (Tektronix TCPA300) are used in the test. The whole test procedure is based on report 5. The pressure of 500g on the skin and the contact area 100mm2 and 10mm2 are designed in the test to obtain more accurate results.

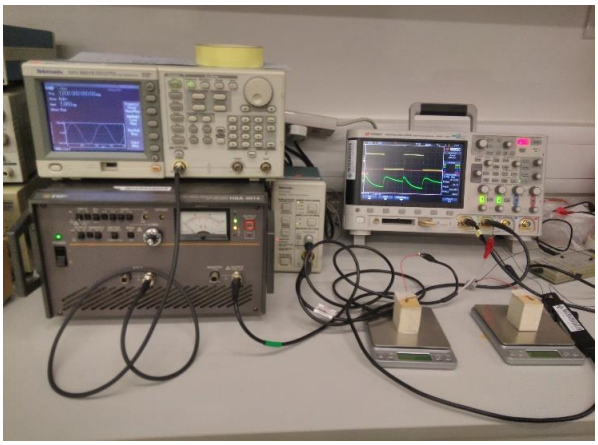


Fig. 3: Test platform

The signal generator and power amplifier are to generate and amplify the signal to obtain the low voltage square wave excitation power source. The digital storage oscilloscope is to measure the voltage and current by using the voltage probe and AC/DC current probe.
The power source for the test is set up as RMS a.c. voltages of 10Vac, 18Vac and 25Vac, Square wave, and nine fixed frequency from 50Hz to 20 kHz. The positive and negative of the power source connect with the line and neutral poles of devices, respectively. The peak value of

**Power Electronics Research Centre, Department of Electrical Engineering, The Hong Kong Polytechnic University, Hong Kong**
**E-mail: 10902353r@connect.polyu.hk**
**E-mail: eric-cheng.cheng@polyu.edu.hk**

test current and pulse time of test current will be measured and recorded. This measured waveform will be analysed and compared to verify the detection criteria. The test platform is shown in Fig. 3.

## III. THE HUMAN IMPEDANCE MODEL ANALYSIS

### *1. Theoretical analysis*

The following analysis would be based on the human model in IEC standard as shown in Fig.1. when the square wave power source is charging the human, especially on the rising edge, the two skin capacitance has been by passed and the current is going through the resistor directly, which has been discribed in the first section.

Therefore, $R_{\text{int}} = \frac{V}{I_{\max}}$ .

when the applied voltage is different, the relative maximum current is different, but the human body's internal impedance is very stable which is close to 1.5 k ohm.

Take XuCD as an example. When the contact area is 100mm$^2$

$$R_{\text{int}} = \frac{\triangle v}{\triangle i} = \frac{v}{I_{\max}} ,$$

When $v$=10V, $i$=6.65mA, when the frequency is 50 Hz. So as the other frequency.

Therefore, when the frequency is at 100, 200, 500, 1k, 2k, 5k, 10k, 20k, the internal resistance is 1.52k, 1.52k, 1.52k, 1.50k, 1.54k, 1.52k, 1.54k, 1.60k, respectively.

The internal resistance of XuCD at all the applied voltages has been illustrated in the Table1.

When the contact area is 10mm$^2$, the internal resistance could be calculated based on the above analysis as shown in Table 2.

The pulse time is determined by the RC constance, the time is chosen by falling to 90% of the maximum current which is close to 2.3 $\tau$ .

Therefore, the total skink capacitance could be calculated by 2.3 $\tau$ =pulse time.

Take XuCD as an example. When the contact area is 100mm$^2$

$\tau$ = Rint x C0, in seconds, where R is the value of the internal resistor in ohms and C is the value of the sum of two skin capacitors in Farads. This then forms the basis of an RC pulse time 2.3$\tau$ can also be thought of as "2.3 x $R_{int}C_0$".

2.3 x $R_{int}C_0$=20.13us, when at frequency of 50 Hz, and the contact area is 100mm$^2$, and the applied voltage is 10V.

It could be seen in the above analysis, the internal resistance could be solved as 1.5 k ohm, therefore, the skin capacitance could be calculated as

$C_0$=20.13us/(2.3× $R_{int}$)=5.8202 nF, So as the other frequency.

Therefore, when the frequency is at 100, 200, 500, 1k, 2k, 5k, 10k, 20k, the skin capacitance is shown in Table 3.

The skin capacitance of XuCD at all the applied voltages has been illustrated in the Table1 when the contact area is 100mm$^2$. As shown in Table 4

When the contact area is 10mm$^2$, the skin capacitance could be calculated based on the above analysis and shown in Table. 5

As we can see, the data is very stable.

### *2. Simulation results*

The simplified model of human being will be as shown in Fig. 4

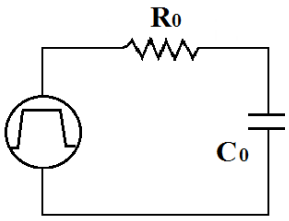



Fig. 4: The simplified model of human being

where $R_0$=$R_{int}$.

Taking XuCD as an example, when the contact area is 100mm$^2$, the average resistance is around 1.54k Ohm.

When the applied voltage is 10V, frequency is 1k, the capacitance is around 5.46nF.

the simulation result will be shown in Fig. 5.

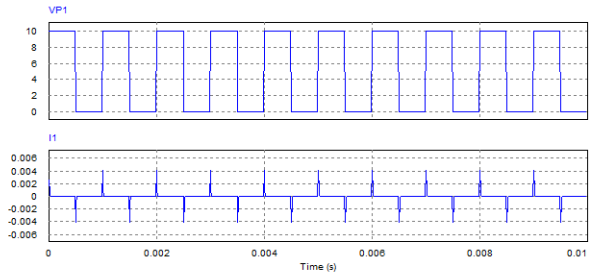



Fig. 5(a): Time response of the square wave source and the input current (simulation result)

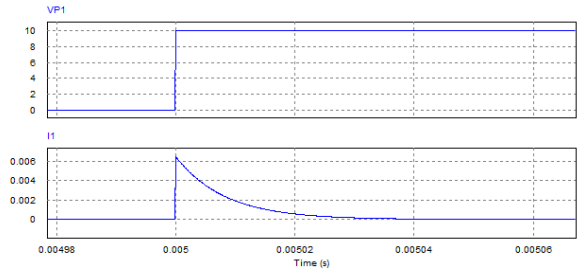



Fig. 5(b): Zoom in of time response of the square wave source and the input current with R=1.54k Ohm, Vin=10V, f=1k Hz, C=5.46nF(simulation result)

**Table 1: Internal resistance with 100mm$^2$ contact area**

| Frequency Hz | 50 | 100 | 200 | 500 | 1k | 2k | 5k | 10k | 20k |
|---|---|---|---|---|---|---|---|---|---|
| 10V | 1.503759 | 1.52207 | 1.52207 | 1.52207 | 1.503759 | 1.540832 | 1.52207 | 1.540832 | 1.642036 |
| 18V | 1.607143 | 1.636364 | 1.607143 | 1.607143 | 1.607143 | 1.607143 | 1.607143 | 1.607143 | 1.698113 |
| 25V | 1.506024 | 1.52439 | 1.436782 | 1.428571 | 1.428571 | 1.436782 | 1.54321 | 1.582278 | 1.666667 |

**Table 2: Internal resistance with 10mm$^2$ contact area**

| Frequency Hz | 50 | 100 | 200 | 500 | 1k | 2k | 5k | 10k | 20k |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | |
| 10V | 2.016129 | 2.083333 | 2.118644 | 2.016129 | 2.083333 | 2.016129 | 2.04918 | 2.083333 | 1.953125 |
| 18V | 1.969365 | 2.097902 | 2.200489 | 2.117647 | 2.179177 | 2.137767 | 2.200489 | 2.117647 | 2.158273 |
| 25V | 2.083333 | 2.04918 | 2.118644 | 2.118644 | 2.155172 | 2.155172 | 2.04918 | 2.04918 | 2.192982 |

**Table 3: The skin capacitance**

| Frequency Hz | 50 | 100 | 200 | 500 | 1k | 2k | 5k | 10k | 20k |
|---|---|---|---|---|---|---|---|---|---|
| | 5.820196 | 5.92157 | 5.9787 | 5.92157 | 5.935848 | 5.680161 | 5.753035 | 5.623726 | 5.014983 |

**Table 4: Skin capacitance with 100mm$^2$ contact area**

| Frequency Hz | 50 | 100 | 200 | 500 | 1k | 2k | 5k | 10k | 20k |
|---|---|---|---|---|---|---|---|---|---|
| 10V | 5.820196 | 5.92157 | 5.9787 | 5.92157 | 5.935848 | 5.680161 | 5.753035 | 5.623726 | 5.014983 |
| 18V | 5.007536 | 5.024396 | 5.115749 | 5.061643 | 5.010242 | 5.007536 | 4.73971 | 4.577391 | 4.152947 |
| 25V | 6.091478 | 6.594226 | 7.232348 | 6.482609 | 6.668261 | 6.324522 | 6.282783 | 5.85287 | 5.191304 |

**Table 5: Skin capacitance with 10mm$^2$ contact area**

| Frequency Hz | 50 | 100 | 200 | 500 | 1k | 2k | 5k | 10k | 20k |
|---|---|---|---|---|---|---|---|---|---|
| 10V | 1.043757 | 0.989217 | 0.952209 | 1.000626 | 0.951652 | 1.004939 | 0.965391 | 0.930783 | 1.119722 |
| 18V | 1.371 | 1.251768 | 1.248734 | 1.299638 | 1.207077 | 1.204019 | 1.189459 | 1.225725 | 1.188551 |
| 25V | 1.235478 | 1.213635 | 1.155374 | 1.112278 | 0.932035 | 0.992557 | 1.239096 | 1.251826 | 1.173704 |

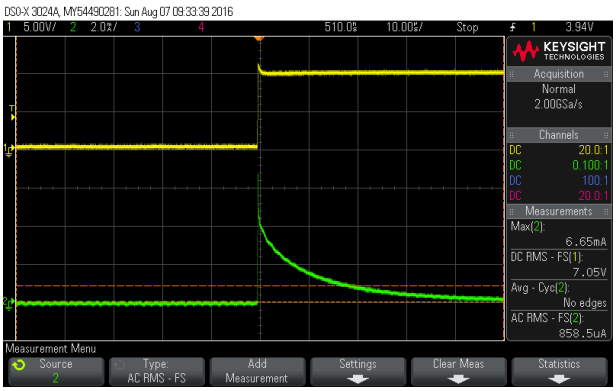



Fig.5(c): Zoom in of time response of the square wave source and the input current (experimental result)

Compare the simulation result with experimental data from the following Table 6., the peak current is 6.57mA and the pulse time is 20.73μs, the two results agree very well with each other, which strongly support the test result of the human impedance and also support that the simplified human model doesn't affect the result.

*3. Comparison with IEC standard*

The unique of the experiment presented is the applied voltage to the human bodies which is square waveform and is different with the standard which is sinewave. Therefore, the standard data could only be the reference.

**Table 6: The experiment results for 8 frequencies of test**

| | contact area=10mm2 | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Peak current (mA) Applied voltage (V) | 50 Hz | 100 Hz | 200 Hz | 500 Hz | 1k Hz | 2k Hz | 5k Hz | 10k Hz |
| 10 | 6.65 | 6.57 | 6.57 | 6.57 | 6.65 | 6.49 | 6.57 | 6.49 |
| 18 | 11.2 | 11 | 11.2 | 11.2 | 11.2 | 11.2 | 11.2 | 11.2 |
| 25 | 16.6 | 16.4 | 17.4 | 17.5 | 17.5 | 17.4 | 16.2 | 15.8 |
| Pulse time (us) Applied voltage(V) | contact area=100mm2 | | | | | | | |
| 10 | 20.13 | 20.73 | 20.93 | 20.73 | 20.53 | 20.13 | 20.14 | 19.93 |
| 18 | 18.51 | 18.91 | 18.91 | 18.71 | 18.52 | 18.51 | 17.52 | 16.92 |
| 25 | 21.1 | 23.12 | 23.9 | 21.3 | 21.91 | 20.9 | 22.3 | 21.3 |

As we can see from the standard as shown in below figure, the human impedance is around 3.2k ohm when the applied voltage is 25V 50 Hz sinewave with large contact area. When the frequency is increased to 2k, the human impedance is close to the internal resistance which is around 600 ohm as shown in figure below. In the experimental results, the human impedance is around 1.5k ohm with 100mm$^2$. With large contact area, the human impedance could be even smaller based on the research. Therefore, the human impedance is smaller than the 3.2k ohm in the standard which verified that the experiment result is consistent with the standard data.

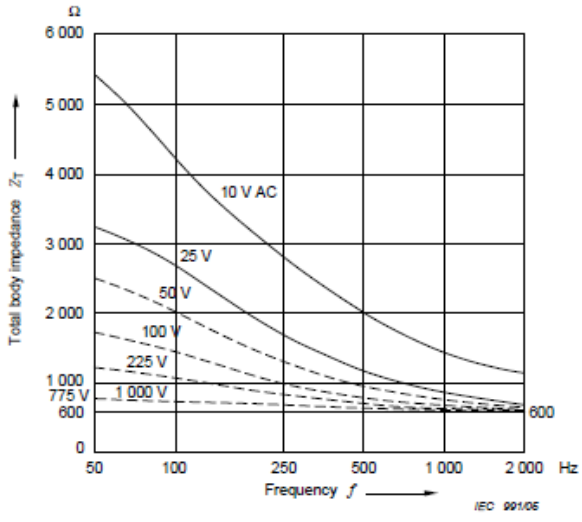



Fig. 6: Frequency dependence of the total body impedance ZT of a population for a percentile rank of 50 % for touch voltages from 10 V to 1 000 V and a frequency range from 50 Hz to 2 kHz for a current path hand to hand or hand to foot, large surface areas of contact in dry conditions

As compared with Fig.6 and 7 in the standard, the human impedance with applied 25V 50 Hz sinewave voltage and 10mm$^2$ and 100mm$^2$ are 200k and 2000k ohm respectively, otherwise in the presented experiment is around 1.5k and 3k ohm respectively. The reason is that in the standard, the applied voltage is low frequency sinewave, the skin

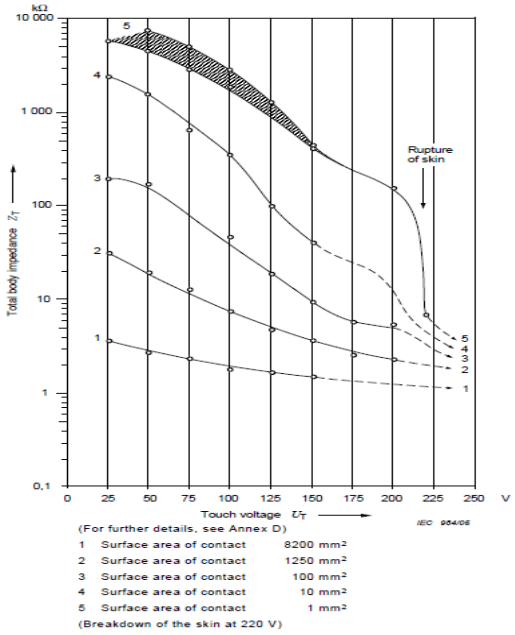



Fig. 7: Dependence of the total impedance ZT of one living person on the surface area of contact in dry condition and at touch voltage (50 Hz)

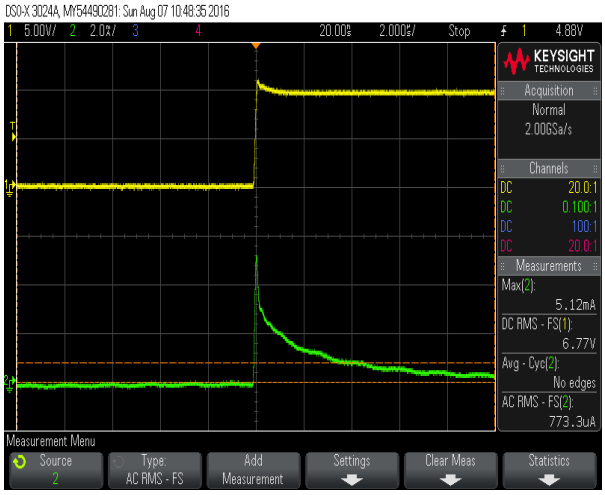
capacitance could not be bypassed, therefore, the skin impedance accounts for most of the human impedance and which is much larger than the internal impedance of the human body.

## IV. Experimental Results

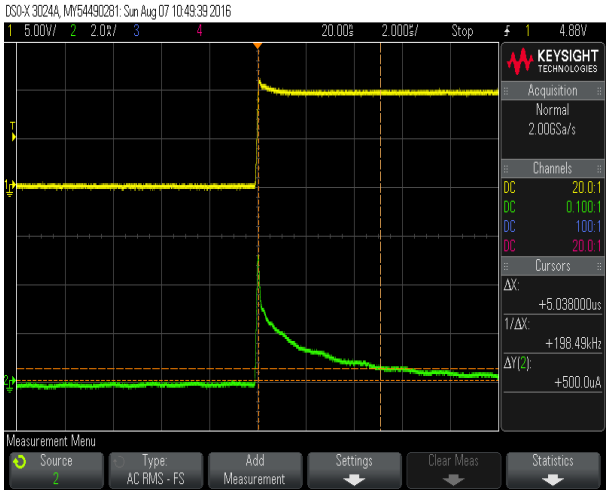
One human being's experimental data would be used to support that simplified RC model could be effectively analyse the data but doesn't affect the result.

In the experiment, the excitation power source is square wave, the voltage level is 10V, 18V and 25V, and frequency is from 50Hz to 20kHz. The pressure applied on the skin is 500g. The contact area is 100mm$^2$ and 10mm2. Fig. 8 Shows the peak current and discharging time of two human bodies are under 10V&50Hz excitation and 10mm$^2$

contact area. The definition of discharging time is when the current from maximum falling to the 90%. The peak current and pulse time has been collected and proceeded with different excitation voltage and frequency. as shown in Fig. 9. The internal resistance and capacitance have been calculated and shown in Fig. 10.

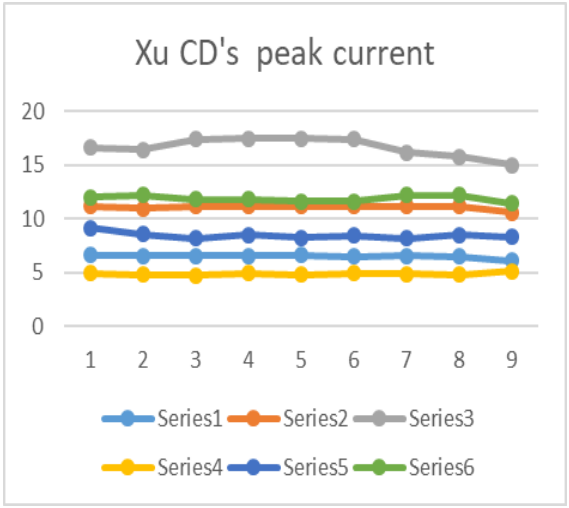



(a) Peak current of Xu CD

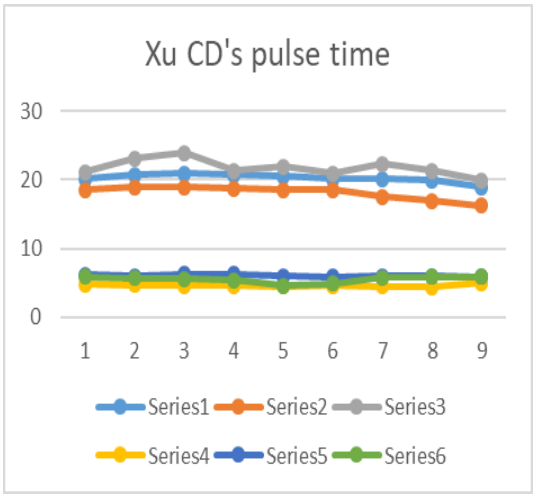



(b) charging time of Xu CD

Fig. 8: Peak current and charging time of XuCD

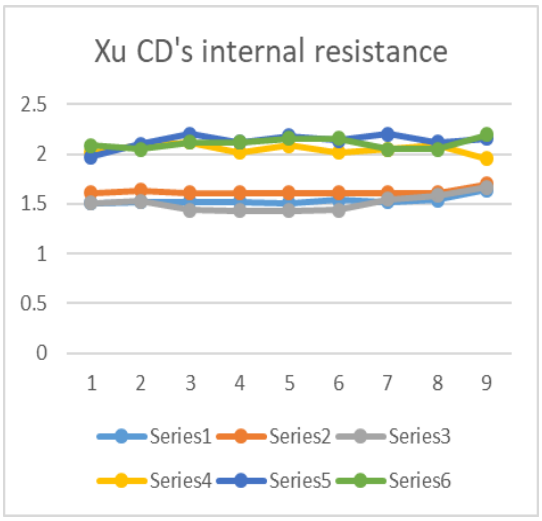



(a)Peak current of Xu CD

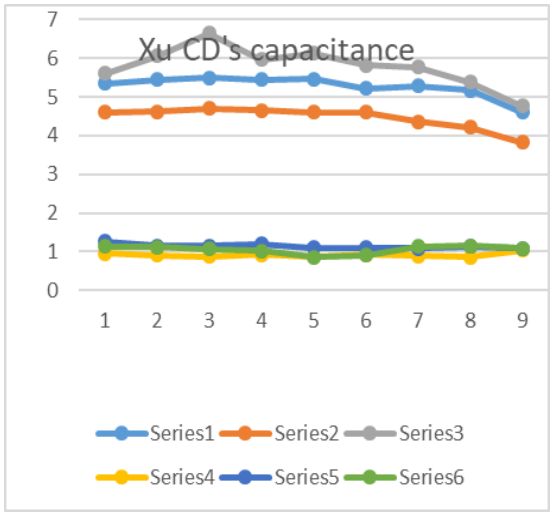



(b) charging time of Xu CD

Fig. 9: Peak current and charging time of XuCD with different excitation voltage and frequency.




(a)Internal resistance of Xu CD




(b)Capacitance of Xu CD

Fig. 10: Internal resistance and the capacitance of human body (nF and x-axis is the frequency changing with 50, 100, 200,500, 1k, 2k, 5k, 10k, 20k Hz)

*1. Peak current and internal resistance*

The peak current is stable for human body for differenct frequency. From a simplified human model, the internal resistor could be calculated and shown in Fig. 10 from $ip=V/R_{int}$, as ip is stable in the different frequencies, Rint is a constanct value and range from 1.4k ohm to 2.2 k ohm. The internal resistance is steady around 1.5k ohm when the contact area is $100mm^2$. When the contact area is $10mm^2$, the internal resistance is steady around 2.0 k ohm with diffrennt frequency, which increase with the contact area decreasing.

*2. The pulse time and capacitance*

The pulse time of the human body are also shown in Fig. 10. The pulse time is constant when the contact area is $10mm^2$. The capacitance could be calculated and shown in Fig. 10. As shown in Fig. 10, the human body's capacitance is increase with the contact area. And when the contact area is 10 $mm^2$, most of human body's capacitance is around 1 nF.

## V. CONCLUSION

A simplified human model was analysed based on IEC standard. By testing 11 human subjects, the relative human body model and parameters could be find. As we can see from the testing result from Fig.9-11, we can know that the internal resistance and capacitance is very stable.

The internal resistance decreases with the contact area increasing, while the capacitance increases with the contact area increasing. Meanwhile, the resistance and capacitance of all human bodies are from 1.2k Ohm to 3.2k Ohm. And in order to obtain an internal resistance close to the real value, voltage with fast step up transient have to be chosen to apply the human body. Therefore, low voltage square wave was applied to human beings. Test results has reviewed human characteristics. Therefore, human can be identified from the other loads by the research.

## REFERENCES


[1] C Gabriel, A Peyman and E H Grant, "Electrical conductivity of tissue at frequencies below 1 MHz", Phys. Med. Biol. 54 , 2009, 4863–4878.

[2] A. van Boxtel, "Skin resistance during square-wave electrical pulsed of 1 to 10 mA", Med. & Biol. Eng. & Comput., 1977, 15, 679-687.

[3] Geojy Mathew, white paper, "Medical Devices Isolation- "How safe is safe enough".

[4] IEC standard TS 60479-1, Effects of current on human beings and livestock –Part 1: General aspects

[5] David T. Lykkem, "Square-wave analysis of skin impedance", Psychophysiology, Vol. No. 2, Sep, 1970, pp262-275.

# Author Index

## Submission Details

Only online submission will be accepted. Please first register and submit online. The paper is in double column and is similar to most IET or IEEE journal format. There is no page limit. Any number of pages of more than 6 will be subject to additional charge.

The paper guidelines can be downloaded using the link: http://perc.polyu.edu.hk/apejournal/

Any queries, please contact Prof. Eric Cheng, Publishing Director of APEJ, Dept. of Electrical Engineering, The Hong Kong Polytechnic University, Hung Hom, Hong Kong. Email: eeecheng@polyu.edu.hk Fax: +852-2330 1544

Any secretarial support and production related matters, please contact Dr. James Ho, Power Electronics Research Centre, The Hong Kong Polytechnic University, Hung Hom, Hong Kong. Email: eeapej@polyu.edu.hk Tel: +852-3400 3348 Fax: +852-3400 3343

## Publication Details

The Journal will be published 2-3 times a year. The first issue was published in 2007. Response time for paper acceptance is within 3 months.

## Financial Charge

All the accepted papers will be printed without charge for 6 or less pages. An additional page charge is HK$100 per page. A hardcopy of the journal will be posted to the corresponding author free of charge. Additional copies of the journal can be purchased at HK$200 each. The charge includes postage and packing.

All Chinese Papers will be subjected to a translational fee of HK$350 per page. It will be charged when the paper is accepted for publication.

## Advertising

Advertisement is welcome. Full page advertisement is HK$1000. For colour advertisement, the amount is doubled. All the advertisement will be both posted online in the journal website and hardcopy of the journal.

For advertising enquiries and details, please contact Ms. Anna Chang, eeapej@polyu.edu.hk .
Tel: +852-3400 3348 Fax: +852-3400 3343

For payment, please send your cheque, payable to 'The Hong Kong Polytechnic University, address to Ms. Kit Chan, Secretary of APEJ, Dept. of Electrical Engineering, The Hong Kong Polytechnic University, Hung Hom, Hong Kong.